VMC is an experimental tool for modelling and analysing (behavioural) variability in product families modelled as Modal Transition Systems (MTSs), written by F. Mazzanti and A. Sulova.

**1. VMC** accepts as input a textual process-algebraic encoding of an MTS and a set of constraints of the form ALTeRnative, EXCludes, REQuires, and IFF.

**2. VMC** can model check whether a product family satisfies a certain property/formula and explain/analyze the result interactively.

**3. VMC** can also visualize a product family/MTS (cf. 5).

**4. VMC** can derive all valid products (LTSs) of a family (MTS + constraints) for further analyses (cf. 4).

**5. VMC** can help understand why a valid product does (not) satisfy a specific verified property by opening a new window for inspecting its encoding (cf. 1) and its visualization.

**VMC** thus allows to interactively explore an MTS of a product family, model check properties (logic formulae) over an MTS, visualize the (interactive) explanations of a verification result, generate all the family's valid products (w.r.t. the given constraints) represented as LTSs, browse and explore these, model check whether they satisfy certain properties, and help understand why a certain valid product does (not) satisfy the verified properties by inspecting it individually.

**VMC** is part of a family of on-the-fly model checkers developed at ISTI-CNR for verifying logic formulae in a CTL-like action- and state-based branching-time temporal logic.

**VMC**'s core holds a command-line version of the model checker and a product generation procedure, both stand-alone executables in Ada (easy to compile for MacOSX/Windows/Linux/Solaris), and is wrapped with a set of CGI scripts handled by a web server, to help graphical html-oriented GUI and integration with LTS minimization / graph drawing tools.

**VMC** is a prototype, publicly usable online; its executables are available upon request.