Static Analysis and Family-based Model Checking with VMC

Maurice H. ter Beek
Franco Mazzanti
ISTI–CNR, Pisa, Italy

Ferruccio Damiani
Luca Paolini
Giordano Scarso
University of Turin, Italy

Michael Lienhardt
ONERA, Palaiseau, France

ABSTRACT

VMC is a research tool for model checking variability-rich behavioural models specified as a modal transition system (MTS) with variability constraints (MTSυ). In this tutorial, we introduce a tool chain built on VMC that allows to perform an efficient kind of family-based model checking in absence of deadlocks. It accepts as input either an MTSυ or a featured transition system (FTS).

CCS CONCEPTS

• **Software and its engineering** → **Software product lines**; **Formal methods**; **Model checking**; **Automated static analysis**.

KEYWORDS

VMC, SPL, variability, FTS, MTS, static analysis, model checking

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Formal models of software product line (SPL) behaviour have been studied extensively throughout the last decade. Such variability-rich behavioural models are typically based on the superimposition in one single labelled transition system (LTS) equipped with feature-based variability (a family model) of multiple LTSs, each of which is a semantic representation of a different variant configuration (a product model). Arguably the best known models are FTSs [8] and MTSυ [3]. An FTS is an LTS whose action-labelled transitions are also labelled with feature expressions that condition the presence of transitions in product models. An MTS is an LTS distinguishing admissible ('may'), necessary ('must'), and optional (may but not must) transitions. An MTSυ is an MTS with an additional set of logical variability constraints akin the feature expressions of FTSs.

The automated analysis of variability models, such as detecting anomalies like dead or false optional features in feature diagrams, has been studied for decades [7]. In [1, 2], efficient automated static analysis of FTSs was introduced to detect behavioural counterparts of such anomalies, like dead transitions that cannot be executed in any product model or, on the contrary, false optional transitions that can be executed in all product models, but also hidden deadlock states that do not deadlock in the family model whereas they do in some product models. The criteria for ambiguities are expressed as propositional formulae, thus reducing ambiguity detection to SAT solving. An FTS can be disambiguated to improve the clarity of the model and to facilitate a kind of family-based analysis.

VMC (https://fmt.isti.cnr.it/vmc) [4, 6] is a research tool for on-the-fly explicit-state model checking of MTSυ properties expressed in a variability-aware action- and state-based branching-time temporal logic v-ACTL [3], which is an action-based version of CTL. VMC offers both product-based model checking, upon explicit generation of the product models, and a kind of family-based model checking. The latter relies on the fact that for properties expressed in v-ACTLive$^{\square}$, which is a rich fragment of v-ACTL interpreted on MTSs without deadlocks, validity for the family model guarantees validity of the property for all product models (cf. [3, Theorem 4]).

FTS4VMC (https://github.com/fts4vmc/FTS4VMC) [5] is a publicly available front-end for VMC which allows to analyse an FTS for ambiguities (dead or false optional transitions and hidden deadlock states), disambiguate an ambiguous FTS, transform an FTS into an MTS, and perform an efficient kind of family-based model checking of such MTS obtained from an FTS without hidden deadlock states.

In this tutorial, the participants are introduced to the field of behavioural variability modelling and analysis; they are made familiar with FTSs, MTSs, and family-based analysis of such models. After explaining ambiguities in FTSs, the participants are introduced to SAT solving and they are shown how to use it for static analysis of FTSs to detect ambiguities. Finally, a tool chain built around VMC is presented and it is demonstrated how to use VMC to perform an efficient kind of family-based model checking of deadlock-free FTSs and MTSs. It is also demonstrated how to use FTS4VMC to detect and remove ambiguities in an FTS, and to transform the resulting FTS into an MTS to make it amenable for analysis with VMC.

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