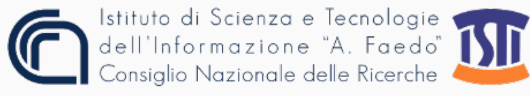
Formal Methods and Tools for Software Product Lines

Maurice ter Beek



joint work with Ferruccio Damiani, Luca Paolini, Giordano Scarso (University of Turin, IT),
Michael Lienhardt (ONERA, FR) and Franco Mazzanti (FMT, CNR–ISTI, Pisa, IT)

UNSAAC, Cusco, Peru, November 30th, 2023

Who am I?

- Member of FMT lab at CNR–ISTI since ’03, lab head since ’19
- MSc (’96) and PhD (’03) degrees from Leiden University (NL)
- Positions in HU (’95-’96,’02), BE (’05), IT (’00-’01), NL (’12-’13,’15)

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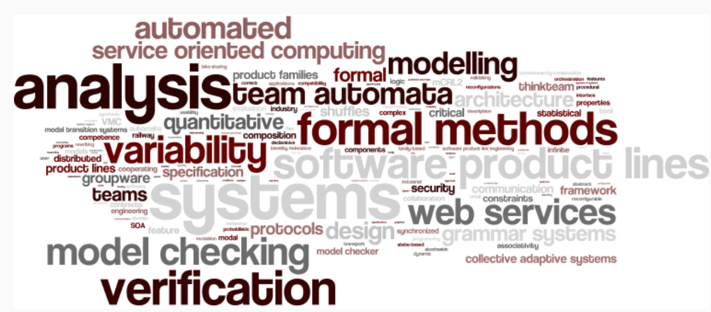
- Formal methods, model checking, SPL, SOC, team automata, railway systems, . . .



Why am I here?

Participation in ICTAC 2023 (UTEC, Lima, next week)

Tutorial on Tuesday, December 5th, 11:00–12:30

Formal Methods and Tools for Software Product Lines

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https://ictac2023.compsust.utec.edu.pe/

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Formal Methods and Tools for Software Product Lines
Maurice ter Beek

Paper on Thursday, December 7th, 16:00–16:30

Realisability of Global Models of Interaction
Maurice ter Beek, Rolf Hennicker, and José Proença

https://ictac2023.compsust.utec.edu.pe/

Outline

Part I

- Software Product Line Engineering (SPLE): variability, features
- Behavioural variability modelling and analysis
    - Product- vs family-based analysis
    - Featured Transition System (FTS)
    - Ambiguities: dead/false optional transitions, hidden deadlocks
- Automated static analysis of FTSs
    - Detecting ambiguities: criteria, SAT solving, implementation
    - Disambiguating FTSs: examples and benchmark experiments

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Part II

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- Model checking principles, temporal logic: LTL, (A)CTL, v-ACTL
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Software Product Line Engineering

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Product Line Engineering in theory. . .

Product Development

Requirements
Product Line Scope
Core Assets
Production Plan

Product Development

Products

Management

. . . and in practice

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- Variability in terms of features
    - Common features that are part of all products
    - Variable features that can be selected per product

Features

- What is a feature?

Features

- What is a feature?
    - End-user visible behaviour or property of a system...

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- What is a feature?
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  - … that may be optional and/or may have alternatives

Features

- What is a feature?
  - End-user visible behaviour or property of a system...
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- Features represent commonalities and variabilities of (software) systems

What's in a *feature*?

Reference	Definition
Kang *et al.* [3]	*"a prominent or distinctive user-visible aspect, quality or characteristic of a software system or systems"*
Kang *et al.* [8]	*"distinctively identifiable functional abstractions that must be implemented, tested, delivered, and maintained"*
Eisenecker and Czarnecki [6]	*"anything users or client programs might want to control about a concept"*
Bosch *et al.* [9]	*"A logical unit of behaviour specified by a set of functional and non-functional requirements."*
Chen *et al.* [10]	*"a product characteristic from user or customer views, which essentially consists of a cohesive set of individual requirements"*
Batory [11]	*"an elaboration or augmentation of an entity(s) that introduces a new service, capability or relationship"*
Batory *et al.* [12]	*"an increment in product functionality"*
Apel *et al.* [13]	*"a structure that extends and modifies the structure of a given program in order to satisfy a stakeholder's requirement, to implement and encapsulate a design decision, and to offer a configuration option."*

Classen *et al.*, What's in a Feature: A Requirements Engineering Perspective @ FASE'08

Feature selection

Typically, only a subset of feature combinations is valid

Figure

Hair

Helmet

optional

mandatory

and

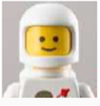
or

xor

$Visor \Rightarrow Helmet$

Product $\Leftrightarrow$ valid feature combination (configuration)

Product ⇔ valid feature combination (configuration)



Product line ⇔ set of valid feature combinations of a domain

Variability models: explicit decisions

- Compact representations of all products of a product family in terms of their features

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- Universal Variability Language (UVL): latest community effort (6th International Workshop on Languages for Modelling Variability: MODEVAR@VaMoS'24)

ter Beek *et al.*, Textual Variability Modeling Languages: An Overview and Considerations @ SPLC'19

Advantages of dedicated conceptual model

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- Transparent decisions, i.e., the originator of a variation point is forced to state the rationale for introducing variability in a specific domain artefact
- Relationships between requirements and variants become traceable (e.g., stakeholders can document which requirements, design, implementation and test artefacts are influenced by a variant)

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- Mandatory variant: if the variation point is selected, this variant *must* always be selected
- Optional variant: if the variation point is selected, this variant *may* be selected but it does not have to be
- Alternative choice, i.e., a collection of at least two optional variants, possibly together with a [min . . . max] notation to indicate the permissible number of variants to be selected: if the variation point is selected, at least "min" variants *must* be selected while at most "max" variants *may* be selected

Variability dependencies (2/2)

Cross-tree constraints

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- Feature attributes (non-functional): $cost(\text{feature}) = 7$, etc.

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- $\mathit{cost}(\text{product}) = \sum\{\mathit{cost}(\text{feature}) \mid \text{feature} \in \text{product}\}$

Example requirements of a coffee machine

1. Initially, a coin must be inserted: either a €, exclusively in case of coffee machines for the European market, or a $, exclusively in case of coffee machines for the Canadian market (alternative features)

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5. As soon as the user has taken her/his beverage, the coffee machine must return in its idle state

Example: coffee machine feature model

optional mandatory alternative or excludes requires

Coffee machine

Sugar s
Beverage b
Ringtone r
Coin o

Cappuccino p
Coffee c
Tea t
Dollar $
Euro €

Example: coffee machine attributed feature model

Automated product derivation

User

Figure

Hair

Helmet

Generator

Mapping

Generated products

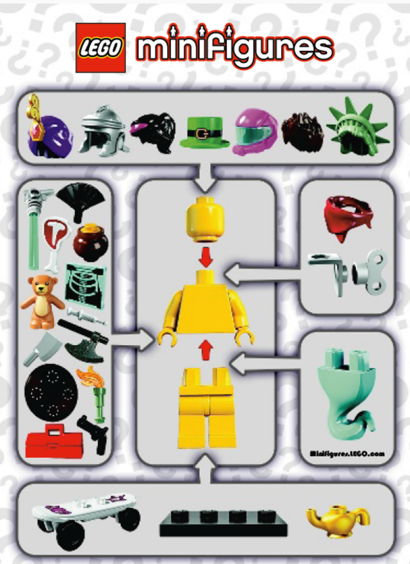
Domain artifacts

Czarnecki & Eisenecker, Generative Programming: Methods, Tools and Applications, 2000

Example: a product line of Lego minifigures

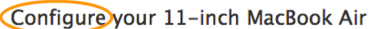
(16 valid feature combinations)

‘Feature model’ for configuring the 16 valid products



(allowing more. . .)

Product lines are everywhere



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Product lines are everywhere

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- Saloon
- Touring
- Convertible
- Coupé
- Gran Turismo
- Sports Hatch
- Roadster
- Sports Activity Coupé
- Sports Activity Vehicle

Number of seats

30 Vehicles (465 Model variants)

1

BMW 1 Series 3-door Sports Hatch (34)
from £ 17,775.00

BMW 1 Series 5-door Sports Hatch (39)
from £ 18,305.00

2

BMW 2 Series Coupé (14)
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3

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from £ 23,550.00

BMW 3 Series Touring (54)
from £ 24,865.00

BMW 3 Series Gran Turismo (39)
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"*We always have 126,000,000 different bicycles in store! (but only the parts for 1,000...)*"

Challenge: scalability is an issue

33 optional, independent features

a unique configuration/variant for every

person on this planet

(examples by C. Kästner, CMU, Pittsburgh, USA)

320 optional, independent features

more configurations/variants than estimated

atoms in the universe

Behavioural variability modelling and analysis

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Software Product Lines (SPL) behaviour

- Configurable (software) system whose variants (products) differ by the provided features, i.e. the functionality that is relevant for an end-user

Feature models

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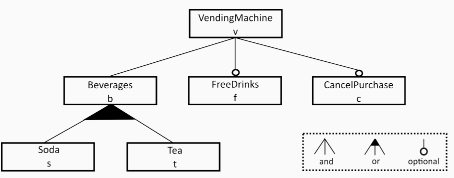

Feature Model (diagram) of a beverage vending machine

Feature models analysis

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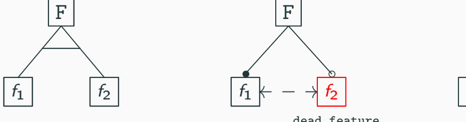

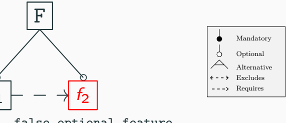

Benavides *et al.*, Automated Analysis of Feature Models 20 Years Later: a Literature Review. *Inf. Syst.*, 2010

Meinicke, Thüm *et al.*, Mastering Software Variability with FeatureIDE, 2017

SPL analysis

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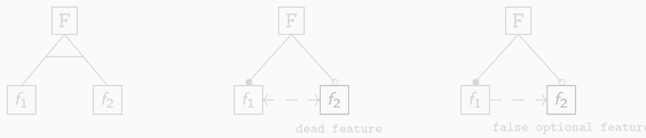

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- Popular in embedded / critical systems domain: formal modelling and analysis techniques to prove SPL behaviour correct are widely studied

  Thüm *et al.*, A classification and survey of analysis strategies for SPLs. *ACM Comput. Surv.*, 2014

- Challenge known formal methods & tools by potentially high number of different variants, each giving rise to a large state space, in general

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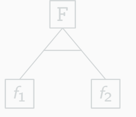
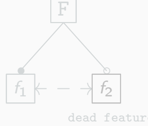
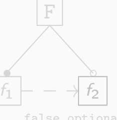
- Configurable (software) system whose variants (products) differ by the provided features, i.e. the functionality that is relevant for an end-user







Benavides *et al.*, Automated Analysis of Feature Models 20 Years Later: a Literature Review. *Inf. Syst.*, 2010

Meinicke, Thüm *et al.*, Mastering Software Variability with FeatureIDE, 2017

- Popular in embedded / critical systems domain: formal modelling and analysis techniques to prove SPL behaviour correct are widely studied

  Thüm *et al.*, A classification and survey of analysis strategies for SPLs. *ACM Comput. Surv.*, 2014

- Challenge known formal methods & tools by potentially high number of different variants, each giving rise to a large state space, in general

⇒ Lift success stories known for single systems (products) to *sets* of products (families) by exploiting variability modelling and analysis

Variability analysis strategies

(type checking, static analysis, model checking, theorem proving, testing, etc.)

Product-Based Analysis

Family-Based Analysis

Feature-Based Analysis

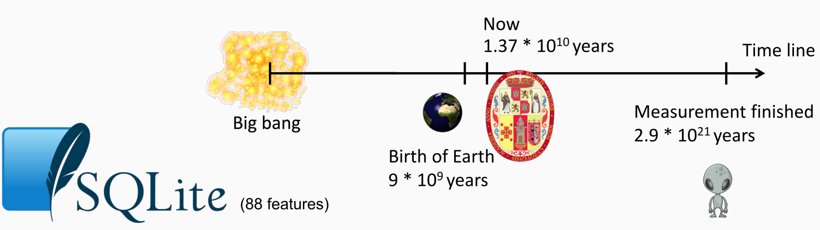
Product-based analysis:

- Simple, brute-force approach
- Make use of standardly available, highly optimised analysis tools

Product-based analysis: inefficient, if not infeasible

- Simple, brute-force approach
- Make use of standardly available, highly optimised analysis tools

- Number of product variants is exponential in number of features
- Same piece of behaviour or code is verified numerous times, as many times as the number of variants that are able to execute it



(example by S. Apel, Saarland University, Germany)

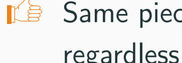
Solution: family-based analysis

Beneficial in case of many products with substantial similarities

Same piece of behaviour (or code) is verified only once, regardless of how many variants can produce it

Solution: family-based analysis

Beneficial in case of many products with substantial similarities

 Same piece of behaviour (or code) is verified only once, regardless of how many variants can produce it

More complex analysis tasks

Requires (compact) family models (superimposed, *150% models*)

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(e.g. FTS,MTSυ, Feature Net, PL-CCS, fLTL, fCTL, v-ACTL, QFLan, SNIP, VMC)

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Dimovski et al., Family-based model checking without a family-based model checker @ SPIN'15
Chrszon *et al.*, Family-based modeling and analysis for probabilistic systems: featuring ProFeat @ FASE'16
ter Beek *et al.*, Family-Based Model Checking with mCRL2 @ FASE'17
Dimovski *et al.*, Variability-specific Abstraction Refinement for Family-based Model Checking @ FASE'17
Dimovski, Abstract Family-Based Model Checking Using Modal Featured Transition Systems @ FASE'18
ter Beek *et al.*, Family-Based SPL Model Checking Using Parity Games with Variability @ FASE'20

Featured Transition Systems (FTSs)

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Part I

- Software Product Line Engineering (SPLE): variability, features
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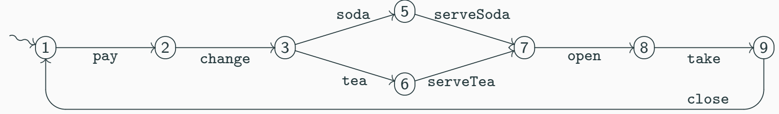
- FTS4VMC toolchain

Labelled Transition System (LTS)

A Labelled Transition System (LTS) is a quadruple (S, Σ, s_0, δ) with states S, actions Σ, initial state s_0, and transitions $\delta \subseteq S \times \Sigma \times S$



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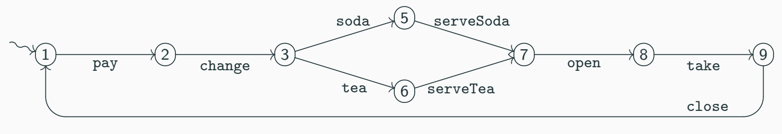


S 1   2   3 $\cdots$ 7   8   9

Σ pay   change $\cdots$ open   take   close

s_0 → 1

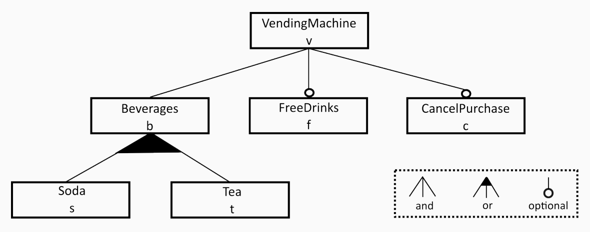
δ 1 —pay→ 2   2 —change→ 3 $\cdots$ 7 —open→ 8   8 —take→ 9

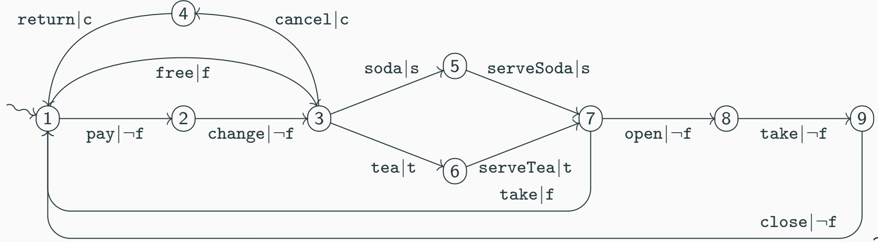
9 —close→ 1

From LTS to FTS

An FTS adds to an LTS a feature model and so-called feature expressions

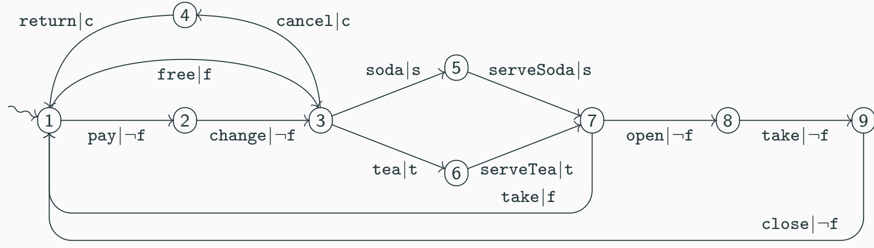
Classen *et al.*, Model checking lots of systems @ ICSE'10, FTSs. *IEEE TSE*, 2013





Featured Transition System (FTS)

A Featured Transition System (FTS) is a sextuple $(S, \Sigma, s_0, \delta, F, \Lambda)$ with states S, actions Σ, initial state s_0, (featured) transitions $\delta \subseteq S \times \Sigma \times \mathbb{B}(F) \times S$, with Boolean (feature) expressions $\mathbb{B}(F)$ over features F, and (product) configurations $\Lambda \subseteq \{ \lambda : F \to \mathbb{B} \}$



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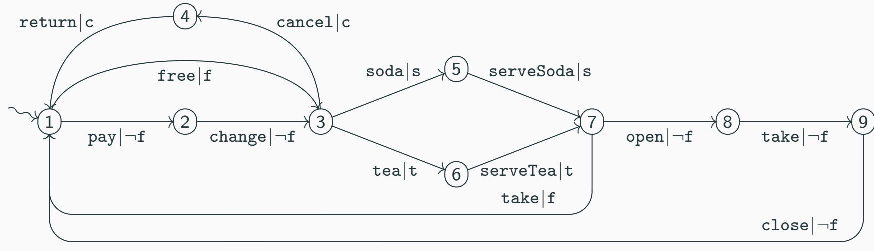

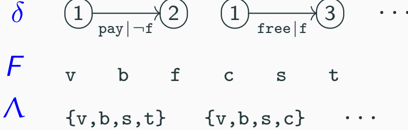

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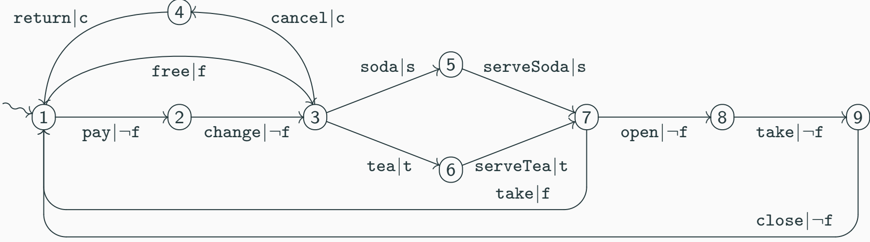
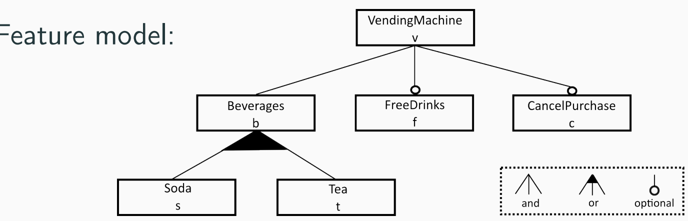


LTS $\mathcal{F}|_\lambda$ specified by configuration $\lambda \in \Lambda$ is called a product of $\mathcal{F}$ [remove: 1) all featured transitions whose feature expressions are not satisfied by λ; 2) all unreachable states and their outgoing transitions]

FTS of example SPL: a vending machine

Feature model:



12 valid products e.g., $\{\texttt{v,b,s,t}\}$, $\{\texttt{v,b,s,c}\}$

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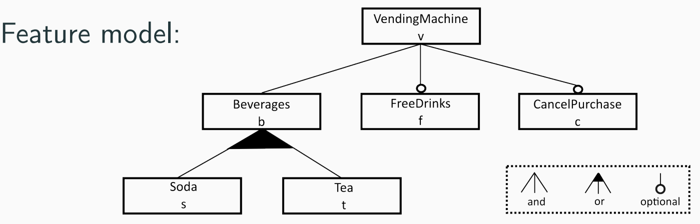
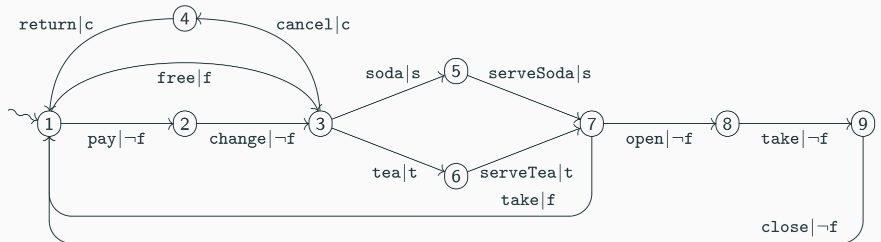


FTS of 12 valid products (LTSs) e.g., $\{v,b,s,t\}$, $\{v,b,s,c\}$



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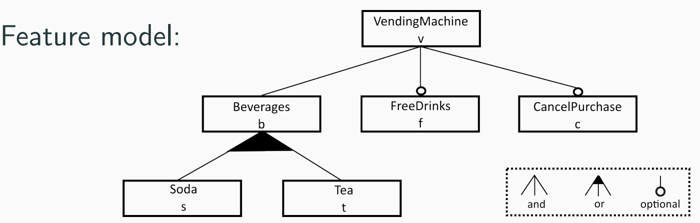
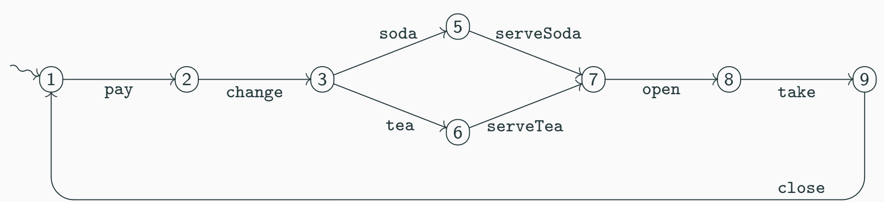
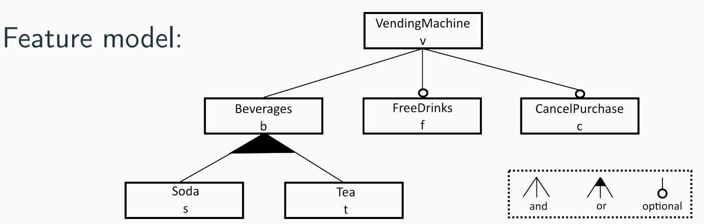


12 valid products (LTSs) e.g., {v,b,s,t}, {v,b,s,c}



FTS of example SPL: a vending machine

Feature model:



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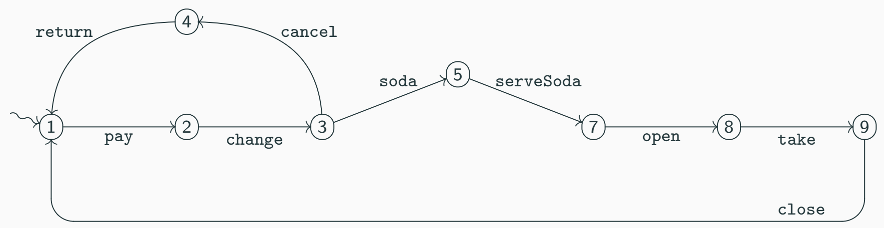

Ambiguities in behavioural models

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Key idea and aim of our SPLC'19 paper

Mimick anomaly detection known from feature model analysis in behavioural SPL models (FTSs) by automated static analysis:

1. dead transitions
2. false optional transitions
3. hidden deadlock states

Key idea and aim of our SPLC'19 paper

Mimick anomaly detection known from feature model analysis in behavioural SPL models (FTSs) by automated static analysis:

1. dead transitions
2. false optional transitions
3. hidden deadlock states

Catch and offer means to remove possible ambiguities in FTSs:

1. Ambiguous FTSs are undesired: provide unclear ideas of the SPLs
2. Unambiguous FTSs pave way to efficient family-based verification

Ambiguous FTS

dead transition

an FTS transition not reachable in any product (LTS)

Ambiguous FTS

dead transition an FTS transition not reachable in any product (LTS)

false optional transition a featured FTS transition which is

1. not dead
2. not annotated with feature expression $\top$ (true, i.e., selected)
3. present in every FTS product in which its source state is present

Ambiguous FTS

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false optional transition a featured FTS transition which is

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3. present in every FTS product in which its source state is present

hidden deadlock state an FTS state which is

1. not a deadlock (i.e., it has outgoing transitions) in the FTS
2. a deadlock (i.e., no outgoing transitions) in some FTS product

---

Deadlock freedom is an important safety property: a system should not reach a state where no further action is possible, thus guaranteeing *progress* or liveness; for configurable systems, this extends to guaranteeing liveness for all system variants (products)

Ambiguous FTS $\longrightarrow$ unambiguous FTS

Transformation:

1. remove dead transitions

Ambiguous FTS $\longrightarrow$ unambiguous FTS

Transformation:

1. remove dead transitions

2. turn false optional transitions into *must* transitions (i.e., labelled with $\top$)

Ambiguous FTS $\longrightarrow$ unambiguous FTS

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1. remove dead transitions
2. turn false optional transitions into *must* transitions (i.e., labelled with $\top$)
3. make hidden deadlock states s explicit:

Step (3) must be performed only for the hidden deadlock states that have not yet become explicit deadlock states upon the removal of dead transitions in step (1)

Ambiguous FTS $\longrightarrow$ unambiguous FTS

Transformation:

1. remove dead transitions

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   3.1 add a deadlock state $s_\dagger \notin S$

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Ambiguous FTS $\longrightarrow$ unambiguous FTS

Transformation:

1. remove dead transitions

2. turn false optional transitions into *must* transitions (i.e., labelled with $\top$)

3. make hidden deadlock states s explicit:

   3.1 add a deadlock state $s_\dagger \notin S$

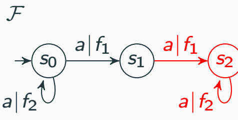
   3.2 $\forall s$: add a *deadlock transition* from s to $s_\dagger$ labelled with $\dagger \notin \Sigma$ and with a feature expression that negates the disjunction of the feature expressions of all outgoing transitions of s

---

Step (3) must be performed only for the hidden deadlock states that have not yet become explicit deadlock states upon the removal of dead transitions in step (1)

Example transformations

Feature Model: $f_1 \oplus f_2$



$\mathcal{F}'$

s_0 —$a \mid \top$→ s_1 —$a \mid f_1$→ s_2; s_0: $a \mid f_2$; s_2: $a \mid f_2$

$\mathcal{F}|_{\lambda_1} = \mathcal{F}'|_{\lambda_1}$

s_0 —a→ s_1 —a→ s_2

$\mathcal{F}|_{\lambda_2}$

s_0: a

$\mathcal{F}'|_{\lambda_2}$

s_0 —a→ s_1; s_0: a

products $\lambda_1 = \{f_1\}$ and $\lambda_2 = \{f_2\}$

Example transformations

Feature Model: $f_1 \oplus f_2$

$\mathcal{F}$: $s_0 \xrightarrow{a|f_1} s_1 \xrightarrow{a|f_1} s_2$, with loops $a|f_2$ on s_0 and $a|f_2$ on s_2

$\mathcal{F}'$: $s_0 \xrightarrow{a|\top} s_1 \xrightarrow{a|f_1} s_2$, with loops $a|f_2$ on s_0 and $a|f_2$ on s_2

$\mathcal{F}|_{\lambda_1} = \mathcal{F}'|_{\lambda_1}$: $s_0 \xrightarrow{a} s_1 \xrightarrow{a} s_2$

$\mathcal{F}|_{\lambda_2}$: s_0 with loop a

$\mathcal{F}'|_{\lambda_2}$: $s_0 \xrightarrow{a} s_1$, with loop a on s_0

products $\lambda_1 = \{f_1\}$ and $\lambda_2 = \{f_2\}$

$\mathcal{F}_*$: $s_0 \xrightarrow{a|f_1} s_1 \xrightarrow{a|\top} s_2$, with loop $a|f_2$ on s_0

$\mathcal{F}'_*$: $s_0 \xrightarrow{a|\top} s_1 \xrightarrow{a|f_1} s_2$, $s_1 \xrightarrow{\dagger|\neg f_1} s_\dagger$, with loop $a|f_2$ on s_0

Efficient static analysis of FTSs

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One-by-one vs all-in-one [recall]

Recall: family-based (all-in-one) analysis

- The analysis of ambiguities for a single SPL's product is an expensive (feasible) task that can be automatised
- To apply the "brute force" by analysing all products of an SPL is too expensive to be used in concrete cases
- However products of an SPL share a common "piece of code", thus analysing each product individually (brute-force analysis) would involve a lot of redundancy

How to leverage this commonality and analyse the whole product line at once, bringing the total analysis time down, is a our goal!

FTS ambiguity detection: NP-complete

FTS ambiguity detection problem is NP-complete: we used a SAT tool!

FTS ambiguity detection: NP-complete

FTS ambiguity detection problem is NP-complete: we used a SAT tool!

- We implemented our algorithm in Z3
- We made our implementation publicly available, including all examples used in the rest of these slides
- Our artefact received the ACM reusable badge:

[SPLC'19]

Z3 is a cross-platform Satisfiability Modulo Theories (SMT) solver (that includes a SAT solver) developed by Microsoft:

- it is freely available under the MIT license
- it supports arithmetic, fixed-size bit-vectors, extensional arrays, datatypes, uninterpreted functions, and quantifiers
- its typical applications are static checking, test-case generation, and predicate abstraction

Examples and benchmark experiments

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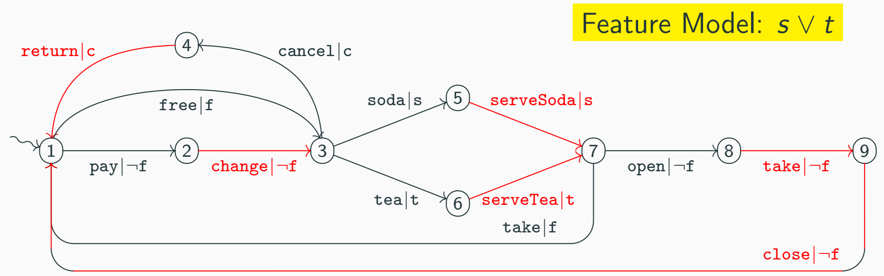
Example static analysis: vending machine



Result of static analysis on FTS

```
Vending Machine: live
 LIVE STATES = [1,2,3,4,5,6,7,8,9]
 DEAD TRANSITIONS = []
 FALSE OPTIONAL TRANSITIONS = [(2,3),(4,1),(5,7),(6,7),(8,9),(9,1)]
 HIDDEN DEADLOCK STATES = []
```

Benchmark experiments (1/3) [EMSE22]

FTS	characteristics			results of static analysis				computational effort	
Model	$\|S\|$	$\|\delta\|$	$\|\Sigma\|$	live-ness	# dead transitions	# false optional transitions	# hidden deadlock states	run-time (s)	memory usage (Mb)
Vending machine Classen, PhD thesis, 2011	9	13	12	yes	0	6	0	0.26	29.765
Coffee machine Asirelli *et al.* @ SPLC'11	14	23	15	yes	0	14	0	0.29	30.305
Soup component Belder *et al.* @ FMSPLE'15	13	28	18	yes	0	7	0	0.316	30.85
Mine pump (system) Classen, PhD thesis, 2011	25	41	22	no	0	25	1	0.344	31.704
Mine pump (controller) Classen, PhD thesis, 2011	77	104	22	no	0	59	4	0.548	36.295
Coffee/Soup machine Belder *et al.* @ FMSPLE'15	182	691	33	yes	8	284	0	37.766	119.427
Mine pump (complete) Classen, PhD thesis, 2011	418	1,255	26	yes	0	308	0	98.994	119.127
Claroline Devroey *et al.* @ VaMoS'14	107	11,236	106	yes	0	259	0	2413.8	2010.229

The experiments were performed on a virtual machine Gentoo 201905, CLI Version VirtualBox (VDI) 64 bit, with 2048 Mb of allocated memory on a Windows 10 Pro 64 bit with 16 Gb of RAM and CPU AMD Ryzen 7 1700X (8 core, 16 threads, 3.4 Ghz)

Benchmark experiments (2/3) [SPLC19] vs. [EMSE22]

FMT
Formal Methods and Tools Lab

FTS	characteristics			computational effort				results
				implementation [SPLC19]		implementation [EMSE22]		
Model	$\|S\|$	$\|\delta\|$	$\|\Sigma\|$	runtime (s)	memory usage (Mb)	runtime (s)	memory usage (Mb)	runtime speedup
Vending machine Classen, PhD thesis, 2011	9	13	12	0.92	38.230	0.26	29.765	3.54x
Coffee machine Asirelli *et al.* @ SPLC'11	14	23	15	2.822	40.140	0.29	30.305	9.72x
Soup component Belder *et al.* @ FMSPLE'15	13	28	18	2.544	40.870	0.316	30.85	8.05x
Mine pump (system) Classen, PhD thesis, 2011	25	41	22	2.192	41.899	0.344	31.704	6.37x
Mine pump (controller) Classen, PhD thesis, 2011	77	104	22	8.12	49.091	0.548	36.295	14.82x
Coffee/Soup machine Belder *et al.* @ FMSPLE'15	182	691	33	timeout	–	37.766	119.427	>7200.00x
Mine pump (complete) Classen, PhD thesis, 2011	418	1,255	26	timeout	–	98.994	119.127	>7200.00x
Claroline Devroey *et al.* @ VaMoS'14	107	11,236	106	timeout	–	2413.8	2010.229	>7200.00x

The experiments were performed on a virtual machine Gentoo 201905, CLI Version VirtualBox (VDI) 64 bit, with 2048 Mb of allocated memory on a Windows 10 Pro 64 bit with 16 Gb of RAM and CPU AMD Ryzen 7 1700X (8 core, 16 threads, 3.4 Ghz)

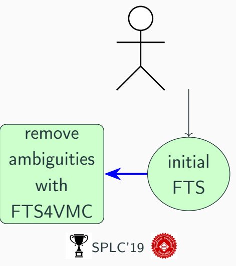
Benchmark experiments (3/3) [liveness only]

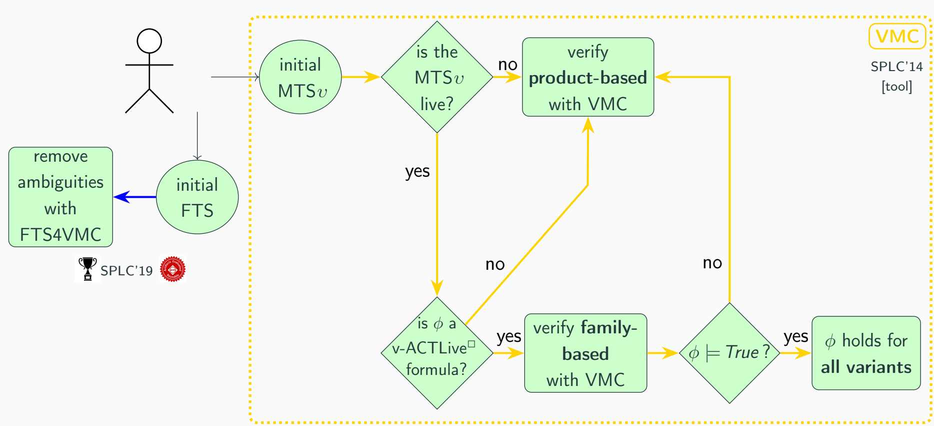
FTS	characteristics			computational effort				results
				full-fledged implementation		specialised implementation		
Model	$\|S\|$	$\|\delta\|$	$\|\Sigma\|$	runtime (s)	memory usage (Mb)	runtime (s)	memory usage (Mb)	runtime fraction
Coffee/Soup machine Belder *et al.* @ FMSPLE'15	182	691	33	37.766	119.427	2.288	61.620	6.06%
Mine pump (complete) Classen, PhD thesis, 2011	417	1,255	26	98.994	119.127	2.948	68.969	2.97%
Claroline Devroey *et al.* @ VaMoS'14	107	11,236	106	2413.8	2010.229	86.752	551.888	3.59%

The experiments were performed on a virtual machine Gentoo 201905, CLI Version VirtualBox (VDI) 64 bit, with 2048 Mb of allocated memory on a Windows 10 Pro 64 bit with 16 Gb of RAM and CPU AMD Ryzen 7 1700X (8 core, 16 threads, 3.4 Ghz)

Wrap up of Part I

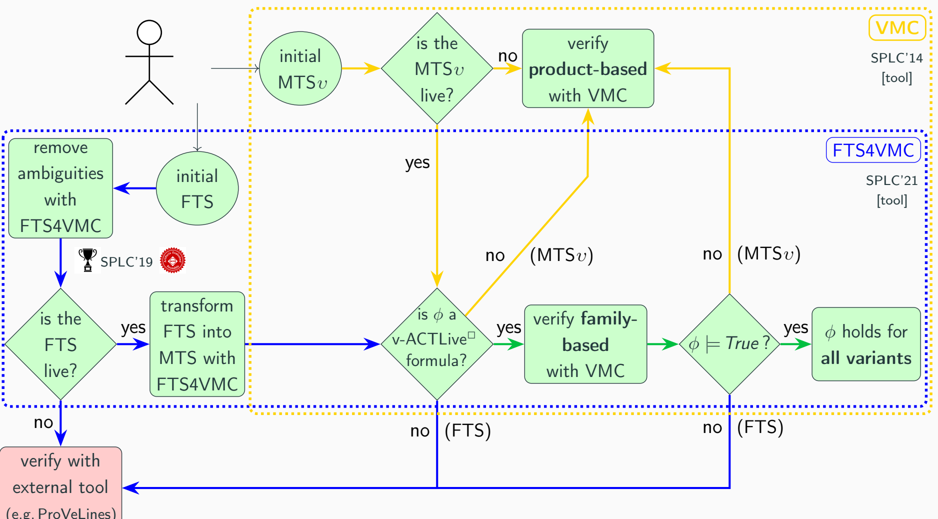
Detect and remove ambiguities





initial MTSυ
is the MTSυ live?
no
verify **product-based** with VMC
VMC
SPLC'14
[tool]
yes
remove ambiguities with FTS4VMC
initial FTS
SPLC'19
no
no
is ϕ a v-ACTLive$^\square$ formula?
yes
verify **family-based** with VMC
$\phi \models$ *True* ?
yes
ϕ holds for **all variants**

FTS4VMC: front-end for VMC: model checking MTSυ/FTS



The FTS4VMC implementation is freely available online: https://github.com/fts4vmc/FTS4VMC

Part II

Modal Transition Systems (MTSs) with variability constraints (MTSv)

Outline [recall]

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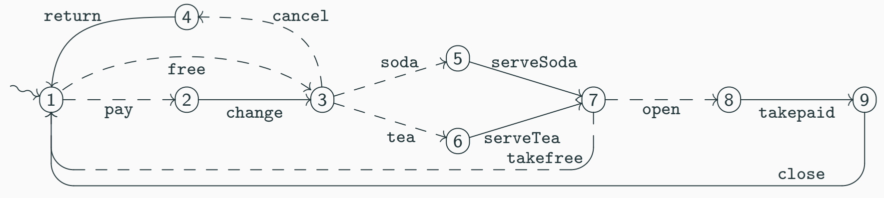
MTSv of example SPL

An MTSv adds to an LTS so-called may and must transitions

+ (variability) constraints

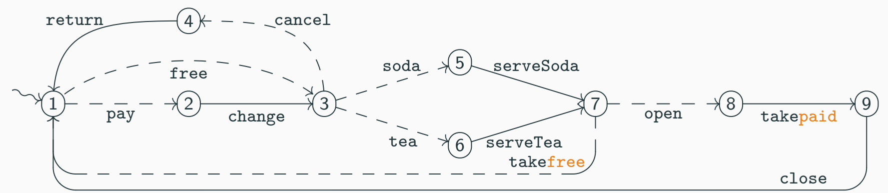
Asirelli *et al.*, Formal Description of Variability in Product Families @ SPLC'11

ter Beek *et al.*, Modelling and analysing variability in product families. *JLAMP*, 2016

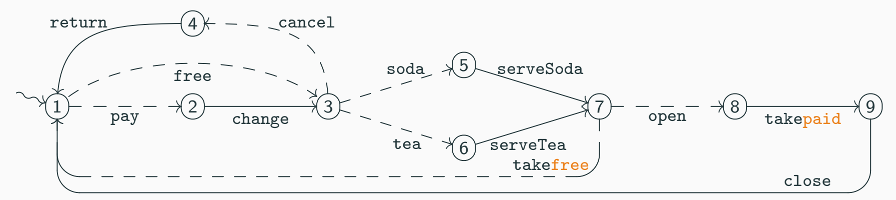


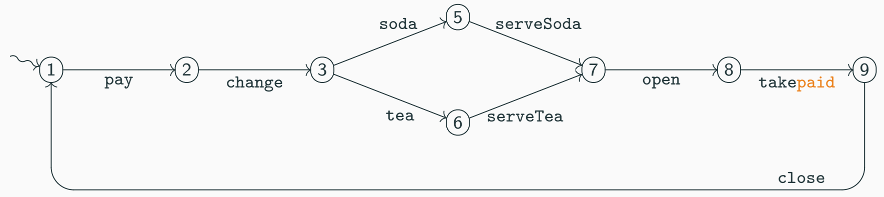

```
Constraints {
 pay ALT free         // precisely one must be present
 soda OR tea          // at least one must be present
 takefree IFF free    // either both or none are present
 open ALT takefree    // precisely one must be present
}
```

Product LTSs of MTSυ of example SPL



Product LTSs of MTSυ of example SPL





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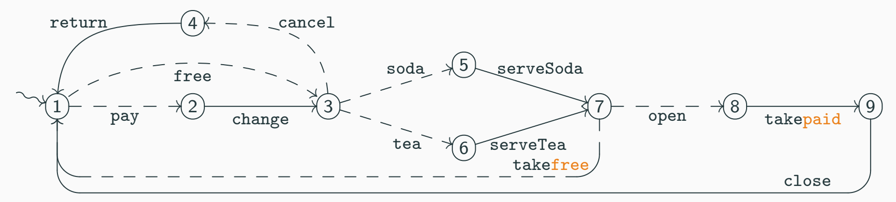

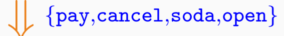

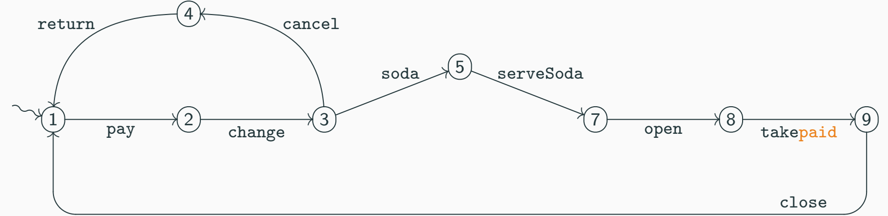

MTSυs are equally expressive as FTSs

Theorem (FTS2MTSυ transformation sound and complete)

Let $\mathcal{F}$ be an FTS and let $\mathcal{M}$ be the MTSυ generated from $\mathcal{F}$ according to the FTS2MTSυ model transformation algorithm.

Then the sets of derived variants $\mathsf{lts}(\mathcal{F})$ and $\mathsf{lts}(\mathcal{M})$ coincide, up to dummy transitions and action relabelling.

ter Beek *et al.*, From FTSs to MTSs with Variability Constraints @ SEFM'15

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ter Beek *et al.*, From FTSs to MTSs with Variability Constraints @ SEFM'15

Theorem (MTSυ2FTS transformation sound and complete)

Let $\mathcal{M}$ be an MTSυ and let $\mathcal{F}$ be the FTS generated from $\mathcal{M}$ according to the MTSυ2FTS model transformation algorithm.

Then $\mathsf{lts}(\mathcal{M}) = \mathsf{lts}(\mathcal{F})$.

ter Beek *et al.*, On the Expressiveness of MTSs with Variability Constraints. *SCP*, 2019

Model checking principles

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What is model checking? [skip]

requirements

Formalizing

property specification

system

Modeling

system model

Model Checking

satisfied

violated + counterexample

Simulation

location error

---

overview taken from Baier & Katoen, *Principles of Model Checking*, MIT, 2008

Model checking process [skip]

Modelling phase:

- model the system under consideration using the model description language of the model checker at hand
- as a first sanity check and quick assessment of the model perform some simulations
- formalise the property to be checked using the property specification language

Running phase:

- run the model checker to check the validity of the property in the system model

Analysis phase:

- property satisfied? $\rightarrow$ check next property (if any)
- property violated? $\rightarrow$
    1. analyse generated counterexample by simulation
    2. refine the model, design or property
    3. repeat the entire procedure
- out of memory? $\rightarrow$ try to reduce the model and try again

Strengths and weaknesses [skip]

- General verification approach, applicable to a wide range of applications (e.g., embedded systems, software engineering, hardware design)
- Supports partial verification, i.e. properties can be checked individually, allowing to focus on essential properties first (no complete requirement specification needed)
- Not vulnerable to likelihood that an error is exposed; this contrasts with testing and simulation that are aimed at tracing the most probable defects
- Provides diagnostic info in case a property is invalidated: very useful for debugging
- **Potentially a "push-button" technology**, requiring neither a high degree of user interaction nor a high degree of expertise
- Enjoys a rapidly increasing interest by industry: several companies have started their in-house verification labs (e.g., Amazon), frequent job offers with required skills in model checking, and commercial model checkers have become available
- Easy integration in existing development cycles: its learning curve is not very steep, empirical studies indicate that it may lead to shorter development times
- Sound and mathematical underpinning, based on theory of graph algorithms, data structures and logic

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Strengths and weaknesses [skip]

- Mainly appropriate to control-intensive applications and less suited for data-intensive applications as data typically ranges over infinite domains
- Applicability subject to decidability issues: for infinite-state systems or reasoning about abstract data types (which requires undecidable or semi-decidable logics), model checking is in general not effectively computable
- Verifies a system model, and not the actual system (product or prototype) itself: **any obtained result is thus as good as the system model** (need complementary techniques, like testing, to find fabrication faults (for HW) or coding errors (for SW)
- Checks only stated requirements, i.e. **no guarantee of completeness**, since the validity of properties that are not checked cannot be judged
- Suffers from state space explosion problem: number of states needed to model the system accurately may easily exceed the amount of available computer memory (despite the development of several very effective methods to combat this problem, models of realistic systems may still be too large to fit in memory)
- Its usage requires some expertise in finding appropriate abstractions to obtain smaller system models and to state properties in the logical formalism used
- Correct results not guaranteed: like any tool, it may contain software defects
- Does not allow checking generalizations: in general, checking systems with an arbitrary number of components, or parameterized systems, cannot be treated

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Temporal logic: LTL, (A)CTL, ν-ACTL

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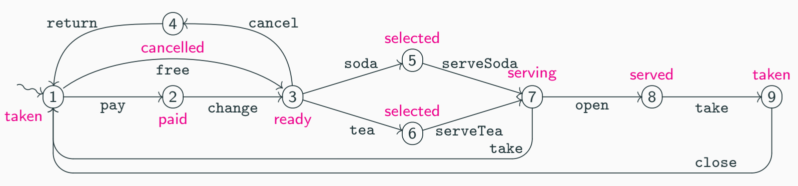
Doubly-Labelled Transition System (L^{2}TS)

A Doubly-Labelled Transition System (L^{2}TS) is a sextuple $(S, \Sigma, s_0, \delta, AP, L)$ in which (S, Σ, s_0, δ) is an LTS, AP is a set of atomic propositions, and $L \colon S \to 2^{AP}$ is a function labelling each state with a set of AP (here singleton)

De Nicola & Vaandrager, Three Logics for Branching Bisimulation. *J. ACM*, 1995

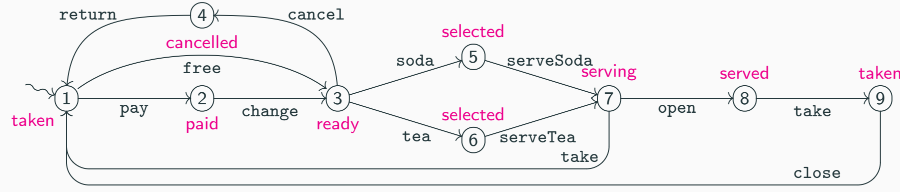


AP paid ready ... served taken

L (2) paid (3) ready ... (8) served (9) taken

Kripke structure: only state labelling, no transition labelling

We have seen that possible system evolutions can be described by a directed graph (LTS, L^2TS, FTS, ...), where nodes and edges may be labelled with properties and events



We can reason on the properties of such graphs by evaluating, starting from the initial state, temporal logic formulas

Temporal logic operators [skip]

Temporal logic formulas are formed by composing temporal operators, the most classical of which are of the form:

ALWAYS	$G\ \phi$, meaning ϕ is Globally true from now on
EVENTUALLY	$F\ \phi$, meaning ϕ is eventually true in the Future
NEXT	$X\ \phi$, meaning ϕ is true in the neXt state
UNTIL	$\phi_1\ U\ \phi_2$, meaning ϕ_2 is eventually true, and Until that point ϕ_1 is always true

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Depending on the formal verification framework, formulas are evaluated:

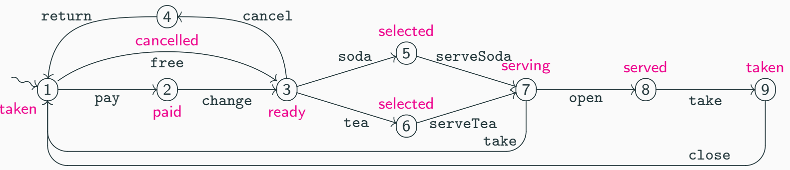
- Independently, on all elements of the set of possible execution sequences, without considering the branching structure of the system evolutions
- Or considering the actual branching structure of the system evolutions

And these operators can refer to just the names of events, to just the properties of states, or to both

Temporal logic operators: linear-time examples

Linear Temporal Logic (LTL)

Pnueli, The temporal logic of programs @ FOCS'77



$G\ (serving \Rightarrow (F\ \ taken))$: for all paths, it is always (globally) true that a state satisfying serving is eventually followed by a (future) state satisfying taken

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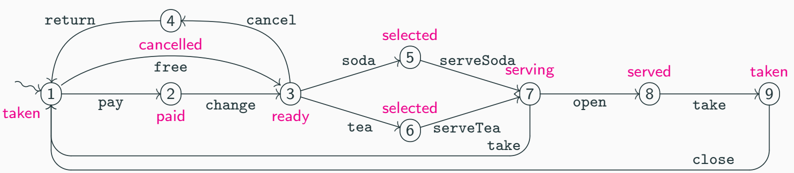


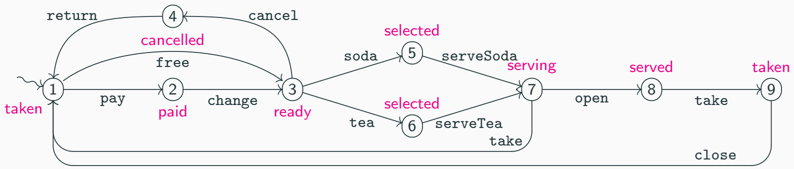
$G\ (serving \Rightarrow (F\ \ taken))$: for all paths, it is always (globally) true that a state satisfying serving is eventually followed by a (future) state satisfying taken

$(F\ \ taken) \Rightarrow (F\ \ serving)$: for all paths, if the path eventually contains a (future) state satisfying taken, then it must contain also a (future) state satisfying serving

Temporal logic operators: branching-time examples

Computation Tree Logic (CTL)

Clarke & Emerson, Design and Synthesis of Synchronization Skeletons Using Branching-Time Temporal Logic @ Logic of Programs Workshop'81

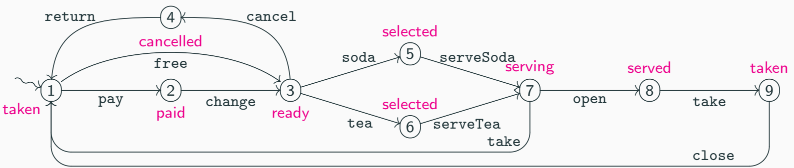


AG EF taken: for all (A) paths it is globally (G) true that there exists (E) a possibility to eventually (F) reach a (future) state satisfying taken

Temporal logic operators: branching-time examples

Action-based Computation Tree Logic (ACTL)

De Nicola & Vaandrager, Three Logics for Branching Bisimulation. *J. ACM*, 1995



$AG\ EF\ taken$: for all (A) paths it is globally (G) true that there exists (E) a possibility to eventually (F) reach a (future) state satisfying taken

$AF_{take \lor cancel}$: all (A) paths eventually (F) lead to a (future) transition for which take or cancel holds

$[pay]\ EX_{change}$: if pay holds for one of the next transitions, then after it, there must exist (E) a next (X) transition for which change holds

$[act]\,\phi$ is a shorthand for $\neg\, EX_{act}\, \neg\phi$

v-ACTL: variability-aware ACTL

ter Beek *et al.*, Modelling and analysing variability in product families. *JLAMP*, 2016

ACTL + dedicated variability-aware versions of temporal operators, e.g.:

$F^{\square}\,\phi$, meaning ϕ is eventually true in the Future, and until that point, all transitions are must transitions

$F^{\square}_{\chi}\,\phi$, meaning the same as $F^{\square}\,\phi$, but that point is reached by executing an action satisfying χ

$X^{\square}\,\phi$, meaning ϕ is true in the neXt state, reached by a must transition

$X^{\square}_{\chi}\,\phi$, meaning the same as $X^{\square}\,\phi$, but that neXt state is reached by a must transition labelled with an action satisfying χ

χ denotes a Boolean composition of actions (transition labels)

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v-ACTLive$^{\square}$ is a specific subset of v-ACTL with the following property: any formula that is true for a live MTS υ, is also true for all product LTSs

---

χ denotes a Boolean composition of actions (transition labels)

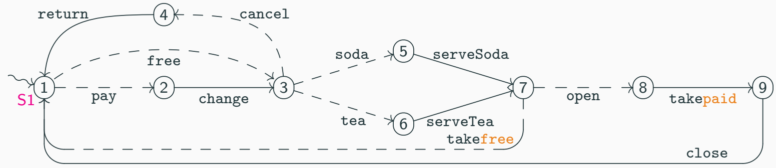
v-ACTLive□:

1. Universal (A) properties that hold for all execution paths (thus also for the subset of MTSυ paths corresponding to a product)
2. Properties that hold for must paths (thus present in all products)
3. Negations of existential (E) properties that do not hold on any path

v-ACTLive$^{\Box}$: family-based model checking with VMC

1. Universal (A) properties that hold for all execution paths (thus also for the subset of MTSv paths corresponding to a product)
2. Properties that hold for must paths (thus present in all products)
3. Negations of existential (E) properties that do not hold on any path

Example v-ACTLive$^{\Box}$ formulas of properties that can thus be verified in a family-based manner with VMC (with a linear complexity)



1. $AG\ AF_{takefree \vee takepaid \vee cancel}\ \top$
2. $[pay]\ EX^{\Box}_{change}$ (also $[pay]\ AX_{change}$, but not $[pay]\ EX_{change}$ seen before)
3. $AG\ [tea]\ \neg E\ [\ _{cancel} U\ \ S1]$

VMC

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Dedicated Variability Model Checker VMC

ter Beek & Mazzanti, VMC @ FM'12, SPLC'14

- VMC is not an industry-ready production/verification tool
- VMC is an academic prototype for research and education

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VMC:

- Part of the KandISTI framework, developed by the FMT lab at CNR–ISTI (https://fmt.isti.cnr.it/kandisti)
- Freely usable online (https://fmt.isti.cnr.it/vmc)
- Command line based executables freely downloadable (Linux, Mac, Windows)
- Available as a local web server for MacOS

Variability analysis strategies supported by VMC

VMC:

- Input models in the form of a set of process-algebraic definitions
- Displays all possible family evolutions in the form of an MTS graph
- Supports a comprehensive temporal logic interpreted on L^2TSs

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VMC offers product- and family-based model checking of MTSυs:

- Allows to verify (some of the) properties such that they hold for all LTS products of the MTS family . . . and to receive feedback when such properties do not hold ('family-based')
- Allows to generate all the valid products of an MTS family . . . and to separately verify properties on them (product-based)

. . . with a linear complexity

Textual model encoding as process definitions

VMC V6.5
(2019)

New Model ...
Load Current Model
Welcome
Quit

Kandinsky 1908

```
1
2  --  VENDING MACHINE  - MTSv version
3
4  S1 = pay(may) .S2
5     | + free(may) .S3
6  S2 = change(must)  .S3
7  S3 = cancel(may) .S4
8     | + soda(may) .S5
9     | + tea(may) .S6
10 S4 = return(must) .S1
11 S5 = serveSoda(must) .S7
12 S6 = serveTea(must) .S7
13 S7 = takefree(may) .S1
14    | + open(may) .S8
15 S8 = takepaid(must) .S9
16 S9 = close(must) .S1
17
18
19 net SYS = S1
20
21 Constraints {
22  pay ALT free
23  soda OR tea
24  takefree IFF free
25  open ALT takefree
26 }
27
28
29
30
31
```

S1 1, close, pay, return, S2 2, free, 4 S4, change, cancel, S3 4, soda, tea, S5 5, 6 S6, serveSoda, serveTea, S7 7, takefree, open, takepaid, S8 8, 9, S9

Vending Machine: family-based model checking

The properties preserved for all LTS products are those that hold for all possible executions—and use a live fragment of the MTSv (live implies no hidden deadlocks!)

Vending Machine: family-based model checking

The properties preserved for all LTS products are those that hold for all possible executions—and use a live fragment of the MTS v (live implies no hidden deadlocks!)

VMC notifies whenever preservation of an analysis result applies:

VMC V6.5
(2019)

Edit Model
View Current Model
Explore the MTS
Draw Family MTS
Generate Products
Welcome
Quit

Kandinsky 1908

The Formula: *AF {serveSoda or (serveTea or cancel)} true*
is TRUE

The formula holds for ALL the MTS variants

(evaluation time= 0.062 sec.)

(total states generated= 8, computations fragments generated= 12, total evaluation time= 0.062 sec.)

ACTL-UCTL-SocL-vACTL

```
AF {serveSoda or serveTea or cancel}
```

Check The Formula | Explain the Result

Vending Machine: explanation of results

VMC explanation for the formula $AG\ [pay]\ AF_{takepaid}\ \top$

VMC V6.5
(2019)

- Edit Model
- View Current Model
- Explore the MTS
- Draw Family MTS
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- Welcome
- Quit

Kandinsky 1908

The formula:
AG [pay] AF {takepaid} true
is FOUND_FALSE in State C1

This happens because the subformula:
[pay] AF {takepaid} true
is already Not Satisfied in State C1

The formula:
[pay] AF {takepaid} true
is FOUND_FALSE in State C1

This happens because
C1 --> C2 {may, pay}
the transition label satisfies the action expression *pay*
but in State C2 the subformula:
AF {takepaid} true **Is Not Satisfied .**

The formula:
AF {takepaid} true
is FOUND_FALSE in State C2

This happens because there is at least one maximal path from C2 in which all transitions DO NOT satisfy the action expression ***takepaid*****.**
For example:
C2 --> C3 {change}
C3 --> C4 {cancel, may}
C4 --> C1 {return}
C1 --> C2 {may, pay} (C2 closes a loop)
is one of the above mentioned failing paths.

S1 1, S2 2, S3 4, S4 4, S5 5, S6 6, S7 7, S8 8, S9 9
pay, free, return, close, change, cancel, soda, tea, serveSoda, serveTea, takefree, open, takepaid

Vending Machine: product-based model checking

VMC lists for each product the action labels of all may transitions that have been preserved (as must transitions) in that product LTS

VMC V6.5
(2019)

New Model ...
Edit Current Model
Explore the MTS
View Current Model
Draw Family MTS
Generate Products
Welcome
Quit

Kandinsky 1908

Evaluation of the formula "[pay] AF {takePaid} true" on all family products

Product		Result
product+CancelPurchase+FreeDrinks+Soda+Tea_12	Formula evaluates	TRUE
product+CancelPurchase+FreeDrinks+Soda_08	Formula evaluates	TRUE
product+CancelPurchase+FreeDrinks+Tea_10	Formula evaluates	TRUE
product+CancelPurchase+FreeDrinks+Tea_10	Formula evaluates	TRUE
product+CancelPurchase+Soda+Tea_06	Formula evaluates	FALSE
product+CancelPurchase+Soda_02	Formula evaluates	FALSE
product+CancelPurchase+Tea_04	Formula evaluates	FALSE
product+FreeDrinks+Soda+Tea_11	Formula evaluates	TRUE
product+FreeDrinks+Soda_07	Formula evaluates	TRUE
product+FreeDrinks+Tea_09	Formula evaluates	TRUE
product+Soda+Tea_05	Formula evaluates	TRUE
product+Soda_01	Formula evaluates	TRUE
product+Tea_03	Formula evaluates	TRUE

Logic Formula for all Products

```
[pay] AF {takePaid} true
```

Check The Formula | Explain the Result

Family-based model checking FTSs

Outline [recall]

Part I

- Software Product Line Engineering (SPLE): variability, features
- Behavioural variability modelling and analysis
  - Product- vs family-based analysis
  - Featured Transition System (FTS)
  - Ambiguities: dead/false optional transitions, hidden deadlocks
- Automated static analysis of FTSs
  - Detecting ambiguities: criteria, SAT solving, implementation
  - Disambiguating FTSs: benchmark experiments

Part II

- Modal Transition System with variability constraints (MTSv)
- Model checking principles, temporal logic: LTL, (A)CTL, v-ACTL
- VMC: family-based model checking of MTSs
- Family-based model checking of FTSs
- FTS4VMC toolchain

Family-based model checking (1/2): v-ACTLive$^\square$

Note

1. Any FTS $\mathcal{F}$ can trivially be transformed into an MTS $\mathcal{F}_{\text{MTS}}$
   (must → necessary transitions, featured → optional transitions,
   all transitions admissible, remove all feature expressions)

2. If the FTS is unambiguous, then the corresponding MTS is live
   (as it has no hidden deadlocks, and all must transitions are necessary)

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FTS4VMC: front-end for VMC (family-based model checking MTSυs and FTSs)

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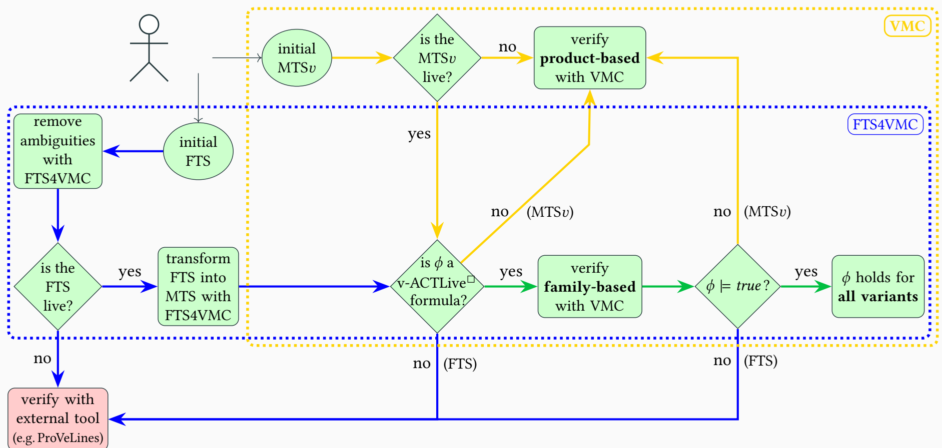
What does it do?

1. Provide a simple UI to work with the proposed toolchain
2. Implements automatic ambiguities removal as shown before
3. Convert unambiguous FTSs into MTSs compatible with VMC

Toolchain: family-based model checking of MTSυs



The green blocks are automated by the toolchain (FTS4VMC+VMC)

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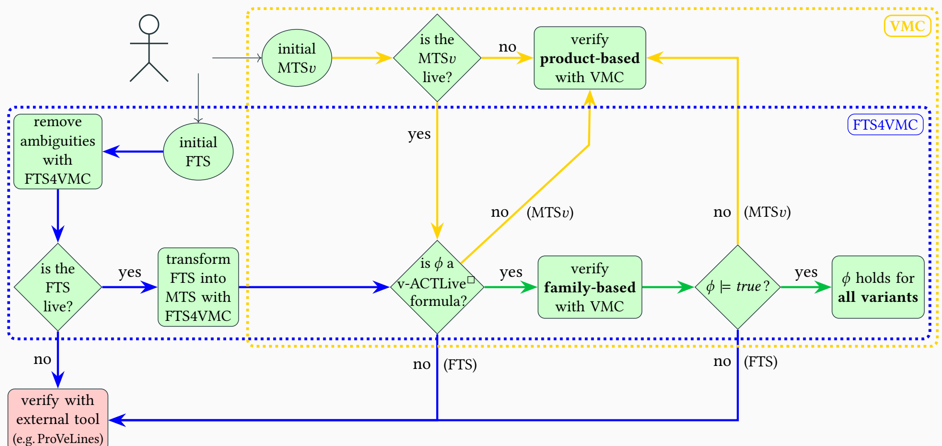
Toolchain: family-based model checking of MTSυs *and* FTSs



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4. Ongoing work:
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Family-based model checking (1/2): v-ACTLive$^{\Box}$ [recall]

FMT Formal Methods and Tools Lab

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Thus:

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Family-based model checking with SPIN . . .

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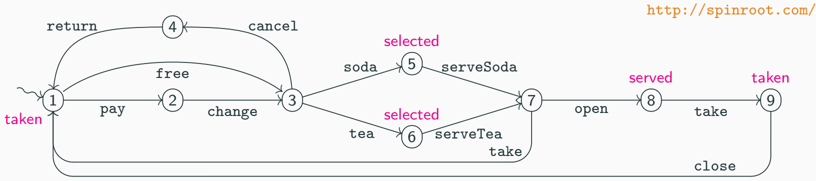

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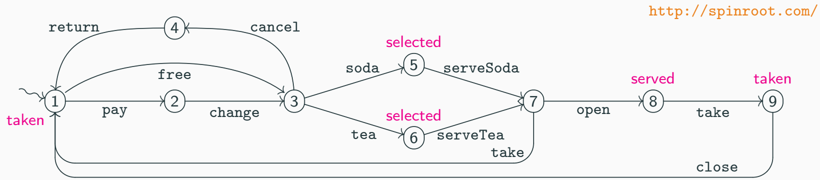

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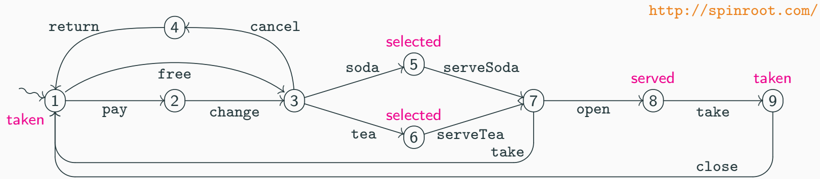

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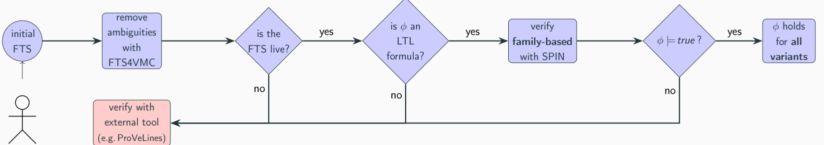

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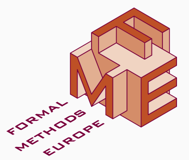
SCP22 M.H. ter Beek, F. Damiani, M. Lienhardt, F. Mazzanti, L. Paolini, and Giordano Scarso, FTS4VMC: A front-end tool for static analysis and family-based model checking of FTSs with VMC. *Science of Computer Programming* 224 (2022), 102879 (original software publication) https://doi.org/10.1016/j.scico.2022.102879

Thanks for your attention!

It would be great to meet some of you at FM 2024:

- Submission: April 19th
- Conference: September 9th–13th
- Co-located: FACS, FMICS, LOPSTR/PPDP, TAP



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